UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,517	12/09/2003	Erik S. Jeng	386998041US	3730

25096 7590 03/24/2005

PERKINS COIE LLP
PATENT-SEA
P.O. BOX 1247
SEATTLE, WA 98111-1247

EXAMINER	
LEE, EUGENE	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 03/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/731,517	JENG, ERIK S.	
	Examiner	Art Unit	
	Eugene Lee	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because (1) it appears on page 7, line 25, that conductive layer 4 should be conductive layer 6; (2) in Figure 2, it is unclear what elements 4, 6a, 6b are pointing to in the figure; and (3) the figures appear to have many unfinished lines that do not line up. For example, in Figure 1, the lines that form the source/drain region 14 are not continuous. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: element 14b (see,

for example, Figure 7). Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities: on page 10, line 26, the word "first" is misspelled, and page 4, line 14, the word "polysilicon" is misspelled .

Appropriate correction is required.

Claim Objections

4. Claims 25, 45, and 52 are objected to because of the following informalities: in line 1 of claim 25, a space is missing in between the limitations "spacer" and "trapping"; in line 6 of claim 25, the limitation "polysilicon" is misspelled; in line 1 of claim 45, the phrase "wherein said" is unnecessarily repeated; and in line 1 of claim 52, a space is missing in between the limitations "Claim" and "28". Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 5, 9, 13, and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Chang et al. 5,969,383. Chang discloses (see, for example, FIG. 1) an NVM cell (nonvolatile memory device) 10 comprising a semiconductor substrate 11, dielectric layer of silicon dioxide layer (gate oxide) 14, gate (gate structure) 16, silicon dioxide layer (first isolation layer) 23, silicon dioxide layers (first spacers) 28, source/drain (source and drain regions) 36, 22, silicide structures (salicide) 42, 44, 46.

Regarding claim 5, see, for example, FIG. 1 wherein Chang discloses a silicon nitride layer (second isolation layer) 24.

Regarding claim 9, see, for example, FIG. 1 wherein Chang discloses nitride spacers (second spacers) 35.

Regarding claim 14, see, for example, FIG. 1 wherein Chang discloses an NVM cell (nonvolatile memory device) 10 comprising a semiconductor substrate 11, dielectric layer of silicon dioxide layer (gate oxide) 14, gate (gate structure) 16, silicon dioxide layer (first isolation layer) 23, nitride spacers (first spacers) 34, 35, source/drain (source and drain regions) 36, 22, silicide structures (salicide) 42, 44, 46.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 2, 3, 6, 7, 10, 11, and 15 thru 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. '383 as applied to claims 1, 5, 9, 13, and 14 above, and further in view of Zheng et al. 6,762,085 B2. Chang does not disclose a pocket implantation region. However, Zheng discloses (see, for example, FIG. 10) a first region 30 comprising an N type source/drain region 9, and a p type halo region (pocket implantation region) 7. In column 3, lines 44-53, Zheng discloses the halo region reducing the risk of punch through, or leakage. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have a pocket implantation region in order to reduce the risk of punch through, or leakage.

Regarding claim 3, Chang does not disclose a lightly doped drain region. However, Zheng discloses (see, for example, FIG. 10) a first region 30 comprising an N type LDD region (lightly doped drain region) 8. It would have been obvious to one of ordinary skill in the art at time of invention to have a lightly doped drain region in order to relax the electric field and reduce leakage current.

Regarding claims 6, and 7, see, for example, FIG. 1 wherein Chang discloses a silicon nitride layer (second isolation layer) 24.

Regarding claim 10, and 11, see, for example, FIG. 1 wherein Chang discloses nitride spacers (second spacers) 35.

Regarding claims 15, 18, and 21, Chang does not disclose the silicide material including $TiSi_2$, $CoSi_2$, or NiSi. However, Zheng discloses (see, for example, FIG. 10, and column 5, lines 27-29) silicide layers 16 comprising titanium silicide, cobalt silicide, and nickel silicide. It would have been obvious to one of ordinary skill in the art at the time of invention to have the silicide material including $TiSi_2$, $CoSi_2$, or NiSi since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice (In re Leshin, 125 USPQ 416) in order to have an adequate conductive material that reduces parasitic resistance.

Regarding claims 17, and 20, see, for example, FIG. 1 wherein Chang discloses an NVM cell (nonvolatile memory device) 10 comprising a semiconductor substrate 11, dielectric layer of silicon dioxide layer (gate oxide) 14, gate (gate structure) 16, silicon dioxide layer (first isolation layer) 23, nitride spacers (first spacers) 34, 35, source/drain (source and drain regions) 36, 22, silicide structures (salicide) 42, 44, 46.

9. Claims 4, 8, 12, and 22 thru 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. '383 as applied to claims 1, 5, 9, 13, and 14 above, and further in view of Kasuya 6,784,078 B2, and further in view of Zheng et al. 6,762,085 B2. Chang does not disclose a double doped drain region. However, Kasuya discloses (see, for example, Fig. 1) a semiconductor device comprising a high concentration impurity diffusion region 44, and a low concentration impurity diffusion region (double doped drain region) 42. It would have been obvious to one of ordinary skill in the art at the time of invention to have a double doped drain region in order to enclose the source/drain region, and reduce leakage current.

Chang in view of Kasuya does not disclose a pocket implantation region. However, Zheng discloses (see, for example, FIG. 10) a first region 30 comprising an N type source/drain region 9, and a p type halo region (pocket implantation region) 7. In column 3, lines 44-53, Zheng discloses the halo region reducing the risk of punch through, or leakage. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have a pocket implantation region in order to reduce the risk of punch through, or leakage.

Regarding claim 8, see, for example, FIG. 1 wherein Chang discloses silicon nitride layer (second isolation layer) 24.

Regarding claim 12, see, for example, FIG. 1 wherein Chang discloses nitride spacers (second spacers) 35.

Regarding claim 23, see, for example, FIG. 1 wherein Chang discloses an NVM cell (nonvolatile memory device) 10 comprising a semiconductor substrate 11, dielectric layer of silicon dioxide layer (gate oxide) 14, gate (gate structure) 16, silicon dioxide layer (first isolation layer) 23, nitride spacers (first spacers) 34, 35, source/drain (source and drain regions) 36, 22, and silicide structures (salicide) 42, 44, 46.

Regarding claim 24, Chang in view of Kasuya does not disclose the silicide material including $TiSi_2$, $CoSi_2$, or NiSi. However, Zheng discloses (see, for example, FIG. 10, and column 5, lines 27-29) silicide layers 16 comprising titanium silicide, cobalt silicide, and nickel silicide. It would have been obvious to one of ordinary skill in the art at the time of invention to have the silicide material including $TiSi_2$, $CoSi_2$, or NiSi since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the

intended use as a matter of obvious design choice (In re Leshin, 125 USPQ 416) in order to have an adequate conductive material that reduces parasitic resistance.

10. Claims 25, 29, 33, 37, 38, and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. 5,969,383 in view of Jeng et al. 6,136,643. Chang discloses (see, for example, FIG. 1) an NVM cell (nonvolatile memory device) 10 comprising a semiconductor substrate 11, dielectric layer of silicon dioxide layer (gate oxide) 14, a gate structure wherein said gate structure comprising a stacked structure including of gate (polysilicon layer) 16, and silicide structure (silicide layer) 42; silicon dioxide layer (second dielectric layer) 23, silicon dioxide layers (first spacers) 28, and source/drain (source and drain regions) 36, 22. Chang does not disclose a first dielectric layer. However, Jeng discloses (see, for example, FIG. 14C) a semiconductor device comprising a polysilicon layer 16A, silicide layer 16B, and cap oxide layer (first dielectric layer) 18. It would have been obvious to one of ordinary skill in the art at the time of invention to have a first dielectric layer in order to protect the silicide structure, and the gate.

Regarding the limitation "polysilicon layer", see column 2, lines 42-44 wherein Chang discloses the gate comprising polycrystalline silicon (polysilicon).

Regarding claim 29, see, for example, FIG. 1 wherein Chang discloses a silicon nitride layer (third dielectric layer) 24.

Regarding claim 33, see, for example, FIG. 1 wherein Chang discloses nitride spacers (second spacers) 35.

Regarding claim 38, Chang discloses (see, for example, FIG. 1) an NVM cell (nonvolatile memory device) 10 comprising a semiconductor substrate 11, dielectric layer of silicon dioxide layer (gate oxide) 14, a gate structure wherein said gate structure comprising a stacked structure including of gate (polysilicon layer) 16, and silicide structure (silicide) 42; silicon dioxide layer (second dielectric layer) 23, nitride spacers (first spacers) 34, 35, and source/drain (source and drain regions) 36, 22.

11. Claims 26, 27, 30, 31, 34, 35, 39, and 41 thru 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. '383 in view of Jeng et al. '643 as applied to claims 25, 29, 33, 37, 38, and 40 above, and further in view of Zheng et al. 6,762,085 B2. Chang in view of Jeng does not disclose a pocket implantation region. However, Zheng discloses (see, for example, FIG. 10) a first region 30 comprising an N type source/drain region 9, and a p type halo region (pocket implantation region) 7. In column 3, lines 44-53, Zheng discloses the halo region reduces the risk of punch through, or leakage. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have a pocket implantation region in order to reduce the risk of punch through, or leakage.

Regarding claim 27, Chang in view of Jeng does not disclose a lightly doped drain region. However, Zheng discloses (see, for example, FIG. 10) a first region 30 comprising an N type LDD region (lightly doped drain region) 8. It would have been obvious to one of ordinary skill in the art at time of invention to have a lightly doped drain region in order to relax the electric field and reduce leakage current. Chang in view of Jeng does not disclose a pocket implantation region. However, Zheng discloses (see, for example, FIG. 10) a first region 30

comprising an N type source/drain region 9, and a p type halo region (pocket implantation region) 7. In column 3, lines 44-53, Zheng discloses the halo region reduces the risk of punch through, or leakage. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have a pocket implantation region in order to reduce the risk of punch through, or leakage.

Regarding claims 30, and 31, see, for example, FIG. 1 wherein Chang discloses silicon nitride layer (third dielectric layer) 24.

Regarding claims 34, and 35, see, for example, FIG. 1 wherein Chang discloses nitride spacers (second spacers) 35

Regarding claims 39, 43, and 47, Chang in view of Jeng does not disclose the silicide material including $TiSi_2$, $CoSi_2$, or NiSi. However, Zheng discloses (see, for example, FIG. 10 and column 5, lines 27-29) silicide layers 16 comprising titianium silicide, cobalt silicide, and nickel silicide. It would have been obvious to one of ordinary skill in the art at the time of invention to have the silicide material including $TiSi_2$, $CoSi_2$, or NiSi since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice (In re Leshin, 125 USPQ 416) in order to reduce parasitic resistance.

Regarding claims 42, and 46, Chang discloses (see, for example, FIG. 1) an NVM cell (nonvolatile memory device) 10 comprising a semiconductor substrate 11, dielectric layer of silicon dioxide layer (gate oxide) 14, a gate structure wherein said gate structure comprising a stacked structure including of gate (polysilicon layer) 16, and silicide structure (silicide) 42;

silicon dioxide layer (second dielectric layer) 23, nitride spacers (first spacers) 34, 35, and source/drain (source and drain regions) 36, 22.

12. Claims 28, 32, 36, and 49 thru 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. '383 in view of Jeng et al. '643 as applied to claims 25, 29, 33, 37, 38, and 40 above, and further in view of Kasuya 6,784,078 B2, and further in view of Zheng et al. 6,762,085 B2. Chang in view of Jeng does not disclose a double doped drain region. However, Kasuya discloses (see, for example, Fig. 1) a semiconductor device comprising a high concentration impurity diffusion region 44 and a low concentration impurity diffusion region (double doped drain region) 42. It would have been obvious to one of ordinary skill in the art at the time of invention to have a double doped drain region in order to enclose the source/drain and reduce leakage current.

Chang in view of Jeng in view of Kasuya does not disclose a pocket implantation region. However, Zheng discloses (see, for example, FIG. 10) a first region 30 comprising an N type source/drain region 9, and a p type halo region (pocket implantation region) 7. In column 3, lines 44-53, Zheng discloses the halo region reduces the risk of punch through, or leakage. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have a pocket implantation region in order to reduce the risk of punch through, or leakage.

Regarding claim 32, see, for example, FIG. 1 wherein Chang discloses silicon nitride layer (third dielectric layer) 24.

Regarding claim 36, see, for example, FIG. 1 wherein Chang discloses nitride spacers (second spacers) 34, 35.

Regarding claim 50, see, for example, FIG. 1 wherein Chang discloses an NVM cell (nonvolatile memory device) 10 comprising a semiconductor substrate 11, dielectric layer of silicon dioxide layer (gate oxide) 14, gate (gate structure) 16, silicon dioxide layer (first isolation layer) 23, nitride spacers (first spacers) 34, 35, source/drain (source and drain regions) 36, 22, silicide structures (salicide) 42, 44, 46.

Regarding claim 51, Chang in view of Jeng does not disclose the silicide material including $TiSi_2$, WSi_2. However, Zheng discloses (see, for example, FIG. 10 and column 5, lines 27-29) silicide layers 16 comprising titianium silicide, and tungsten silicide. It would have been obvious to one of ordinary skill in the art at the time of invention to have the silicide material including $TiSi_2$, WSi_2 since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice (In re Leshin, 125 USPQ 416) in order to reduce parasitic resistance.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eugene Lee
March 14, 2005